



INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

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| (21) International Application Number: PCT/US99/29416 (22) International Filing Date: 10 December 1999 (10.12.1999) (30) Priority Data: 09/215,404 18 December 1998 (18.12.1998) US (60) Parent Application or Grant BOURNS, INC. [/]; O. BARRETT, Andrew, Brian [/]; O. HOGGE, Steven, D. [/]; O. LI, Wen, Been [/]; O. YANG, Kun, Ming [/]; O. KLEIN, Howard, J. ; O. | Published | |
| (54) Title: IMPROVED CONDUCTIVE POLYMER DEVICE AND METHOD FOR MANUFACTURING SAME (54) Titre: DISPOSITIF AMELIORE A POLYMERES CONDUCTEURS ET SON PROCEDE DE FABRICATION | | |
| (57) Abstract <p>An electronic device has three conductive polymer layers sandwiched between two external electrodes and two internal electrodes. The electrodes are staggered to create a first set of electrodes, in contact with a first terminal, alternating with a second set of electrodes in contact with a second terminal. The device is manufactured by: (1) providing (a) a first laminated substructure comprising a first polymer layer between first and second metal layers, (b) a second polymer layer, and (c) a second laminated substructure comprising a third polymer layer between third and fourth metal layers; (2) isolating selected areas of the second and third metal layers to form, respectively, first and second arrays of internal metal strips; (3) laminating the first and second laminated substructures to opposite surfaces of the second conductive polymer layer to form a laminated structure; (4) isolating selected areas of the first and fourth metal layers to form, respectively, first and second arrays of external metal strips; (5) forming insulation areas on the exterior surfaces of the external metal strips; and (6) forming a plurality of first terminals, each electrically connecting a metal strip in the first internal array to a metal strip in the second external array, and a plurality of second terminals, each electrically connecting a metal strip in the first external array to a metal strip in the second internal array; and (7) singulating the laminated structure into a plurality of devices, each having three polymer layers connected in parallel between first and second terminals.</p> (57) Abrégé <p>L'invention porte sur un dispositif électronique présentant trois couches de polymères conducteurs comprises entre deux électrodes extérieures et deux électrodes intérieures. Les électrodes sont séparées de manière à créer un premier ensemble d'électrodes en contact avec une première borne, et un deuxième ensemble d'électrodes alternant, en contact avec une deuxième borne. La fabrication du dispositif se déroule ainsi: (1) constitution: (a) d'une première substructure laminée comportant une première couche de polymère comprise entre une première et une deuxième couche métallique, (b) d'une deuxième couche de polymère, et (c) d'une deuxième substructure laminée comportant une troisième couche de polymère comprise entre une troisième couche métallique et une quatrième; (2) isolement de zones sélectionnées de la troisième couche métallique et de la quatrième de manière à former un premier et un deuxième réseau de bandes métalliques intérieures; (3) laminage d'une première substructure laminées et d'une deuxième sur les faces opposées de la deuxième couche de polymère pour former une structure laminée; (4) isolement de zones sélectionnées de la première couche métallique et de la quatrième pour y former respectivement un premier et un deuxième réseau de bandes métalliques extérieures; (5) formation de zones isolées sur les surfaces extérieures des bandes métalliques extérieures; (6) formation de plusieurs premières bornes reliant chacune électriquement une bande métallique du premier réseau intérieur à une à bande métallique du deuxième réseau extérieur; et (7) découpage de la structure laminée en plusieurs dispositifs présentant chacun trois couches de polymère montées en parallèle entre une première borne et une deuxième.</p> | | |

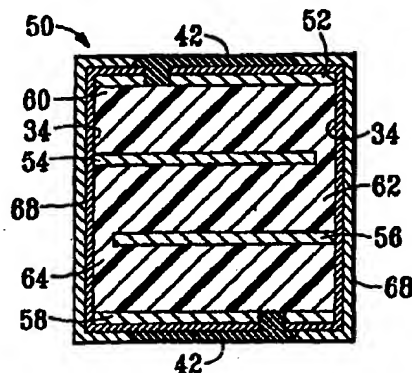
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| (21) International Application Number: PCT/US99/29416 (22) International Filing Date: 10 December 1999 (10.12.99) (30) Priority Data: 09/215,404 18 December 1998 (18.12.98) US (71) Applicant: BOURNS, INC. [US/US]; 1200 Columbia Avenue, Riverside, CA 92507 (US). (72) Inventors: BARRETT, Andrew, Brian; 16 The Downs, Dou- glas, Cork (IE). HOGGE, Steven, D.; 230 Wingfoot Drive, Aptos, CA 95003 (US). LI, Wen, Been; 4F, 6, Alley 2, Lane 194, Taipei (TW). YANG, Kun, Ming; 7F, 28-6, Jung An 15 Street, Chung Li (TW). (74) Agents: KLEIN, Howard, J. et al.; Klein & Szekeres, LLP, Suite 700, 4199 Campus Drive, Irvine, CA 92612 (US). | | | (81) Designated States: AE, AL, AM, AT, AT (Utility model), AU, AZ, BA, BB, BG, BR, BY, CA, CH, CN, CR, CU, CZ, CZ (Utility model), DE, DE (Utility model), DK, DK (Utility model), DM, EE, EE (Utility model), ES, FI, FI (Utility model), GB, GD, GE, GH, GM, HR, HU, ID, IL, IN, IS, JP, KE, KG, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MD, MG, MK, MN, MW, MX, NO, NZ, PL, PT, RO, RU, SD, SE, SG, SI, SK, SK (Utility model), SL, TJ, TM, TR, TT, UA, UG, UZ, VN, YU, ZA, ZW, ARIPO patent (GH, GM, KE, LS, MW, SD, SL, SZ, TZ, UG, ZW), Eurasian patent (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European patent (AT, BE, CH, CY, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE), OAPI patent (BF, BI, CF, CG, CI, CM, GA, GN, GW, ML, MR, NE, SN, TD, TG). Published With international search report. |
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Descripti n

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IMPROVED CONDUCTIVE POLYMER DEVICE
AND METHOD OF MANUFACTURING SAME
CROSS-REFERENCE TO RELATED APPLICATIONS

This application is a Continuation-in-Part of co-pending application Serial No. 09/035,196; filed March 5, 1998.

FEDERALLY SPONSORED RESEARCH OR DEVELOPMENT

Not Applicable

BACKGROUND OF THE INVENTION

The present invention relates generally to the field of conductive polymer positive temperature coefficient (PTC) devices. More specifically, it relates to conductive polymer PTC devices that are of laminar construction, with more than a single layer of conductive polymer PTC material, and that are especially configured for surface-mount installations.

Electronic devices that include an element made from a conductive polymer have become increasingly popular, being used in a variety of applications. They have achieved widespread usage, for example, in overcurrent protection and self-regulating heater applications, in which a polymeric material having a positive temperature coefficient of resistance is employed. Examples of positive temperature coefficient (PTC) polymeric materials, and of devices incorporating such materials, are disclosed in the following U.S. patents:

3,823,217 - Kampe
4,237,441 - van Konynenburg
4,238,812 - Middleman et al.
4,317,027 - Middleman et al.
4,329,726 - Middleman et al.
4,413,301 - Middleman et al.
4,426,633 - Taylor

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- 1 4,445,026 - Walker
- 2 4,481,498 - McTavish et al.
- 3 4,545,926 - Fouts, Jr. et al.
- 4 4,639,818 - Cherian
- 5 4,647,894 - Ratell
- 6 4,647,896 - Ratell
- 7 4,685,025 - Carlomagno
- 8 4,774,024 - Deep et al.
- 9 4,689,475 - Kleiner et al.
- 10 4,732,701 - Nishii et al.
- 11 4,769,901 - Nagahori
- 12 4,787,135 - Nagahori
- 13 4,800,253 - Kleiner et al.
- 14 4,849,133 - Yoshida et al.
- 15 4,876,439 - Nagahori
- 16 4,884,163 - Deep et al.
- 17 4,907,340 - Fang et al.
- 18 4,951,382 - Jacobs et al.
- 19 4,951,384 - Jacobs et al.
- 20 4,955,267 - Jacobs et al.
- 21 4,980,541 - Shafe et al.
- 22 5,049,850 - Evans
- 23 5,140,297 - Jacobs et al.
- 24 5,171,774 - Ueno et al.
- 25 5,174,924 - Yamada et al.
- 26 5,178,797 - Evans
- 27 5,181,006 - Shafe et al.
- 28 5,190,697 - Ohkita et al.
- 29 5,195,013 - Jacobs et al.

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1 5,227,946 - Jacobs et al.
2 5,241,741 - Sugaya
10 3 5,250,228 - Baigrie et al.
4 5,280,263 - Sugaya
5 5,358,793 - Hanada et al.

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6 One common type of construction for conductive polymer PTC devices
7 is that which may be described as a laminated structure. Laminated
8 conductive polymer PTC devices typically comprise a single layer of
9 conductive polymer material sandwiched between a pair of metallic electrodes,
10 the latter preferably being a highly-conductive, thin metal foil. See, for
11 example, U.S. Patents Nos. 4,426,633 - Taylor; 5,089,801 - Chan et al.;
12 4,937,551 - Plasko; 4,787,135 - Nagahori; 5,669,607 - McGuire et al.; and
25 13 5,802,709 - Hogge et al.; and International Publication Nos. WO97/06660 and
14 WO98/12715.

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15 A relatively recent development in this technology is the multilayer
16 laminated device, in which two or more layers of conductive polymer material
17 are separated by alternating metallic electrode layers (typically metal foil),
18 with the outermost layers likewise being metal electrodes. The result is a
35 19 device comprising two or more parallel-connected conductive polymer PTC
20 devices in a single package. The advantages of this multilayer construction
21 are reduced surface area ("footprint") taken by the device on a circuit board,
40 22 and a higher current-carrying capacity, as compared with single layer devices.

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23 In meeting a demand for higher component density on circuit boards,
24 the trend in the industry has been toward increasing use of surface mount
45 25 components as a space-saving measure. Surface mount conductive polymer
26 PTC devices heretofore available have been generally limited to hold currents
27 below about 2.5 amps for packages with a board footprint that generally
50 28 measures about 9.5 mm by about 6.7 mm. Recently, devices with a footprint
29 of about 4.7 mm by about 3.4 mm, with a hold current of about 1.1 amps, have

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1 become available. Still, this footprint is considered relatively large by current
2 surface mount technology (SMT) standards.

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3 The major limiting factors in the design of very small SMT conductive
4 polymer PTC devices are the limited surface area and the lower limits on the
5 resistivity that can be achieved by loading the polymer material with a
6 conductive filler (typically carbon black). The fabrication of useful devices
7 with a volume resistivity of less than about 0.2 ohm-cm has not been practical.
8 First, there are difficulties inherent in the fabrication process when dealing
9 with such low volume resistivities. Second, devices with such a low volume
10 resistivity do not exhibit a large PTC effect, and thus are not very useful as
11 circuit protection devices.

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12 The steady state heat transfer equation for a conductive polymer PTC
13 device may be given as:

$$14 \quad (1) \quad 0 = [I^2 R(f(T_d))] - [U(T_d - T_a)],$$

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15 where I is the steady state current passing through the device; $R(f(T_d))$ is the
16 resistance of the device, as a function of its temperature and its characteristic
17 "resistance/temperature function" or "R/T curve"; U is the effective heat
18 transfer coefficient of the device; T_d is temperature of the device; and T_a is the
19 ambient temperature.

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20 The "hold current" for such a device may be defined as the value of I
21 necessary to trip the device from a low resistance state to a high resistance
22 state. For a given device, where U is fixed, the only way to increase the hold
23 current is to reduce the value of R.

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24 The governing equation for the resistance of any resistive device can be
25 stated as

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$$26 \quad (2) \quad R = \rho L / A,$$

27 where ρ is the volume resistivity of the resistive material in ohm-cm, L is the
28 current flow path length through the device in cm, and A is the effective cross-
29 sectional area of the current path in cm^2 .

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1 Thus, the value of R can be reduced either by reducing the volume
2 resistivity ρ , or by increasing the cross-sectional area A of the device.

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3 The value of the volume resistivity ρ can be decreased by increasing
4 the proportion of the conductive filler loaded into the polymer. The practical
5 limitations of doing this, however, are noted above.

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6 A more practical approach to reducing the resistance value R is to
7 increase the cross-sectional area A of the device. Besides being relatively easy
8 to implement (from both a process standpoint and from the standpoint of
9 producing a device with useful PTC characteristics), this method has an
10 additional benefit: In general, as the area of the device increases, the value of
11 the heat transfer coefficient also increases, thereby further increasing the value
12 of the hold current.

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13 In SMT applications, however, it is necessary to minimize the effective
14 surface area or footprint of the device. This puts a severe constraint on the
15 effective cross-sectional area of the PTC element in the device. Thus, for a
16 device of any given footprint, there is an inherent limitation in the maximum
17 hold current value that can be achieved. Viewed another way, decreasing the
18 footprint can be practically achieved only by reducing the hold current value.

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19 There has thus been a long-felt need for SMT conductive polymer PTC
20 devices that have very small footprints while achieving relatively high hold
21 currents. Applicant's co-pending application Serial No. 09/035,196 (the
22 disclosure of which is incorporated herein by reference) discloses a multilayer
23 SMT conductive polymer PTC device that meets these criteria, as well as a
24 method for fabricating such a device. More efficient and economical methods
25 of manufacturing such devices have, nevertheless, been sought. Furthermore,
26 even higher hold currents for a given footprint continue to be desired.

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27 SUMMARY OF THE INVENTION

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28 Broadly, the present invention is a conductive polymer PTC device that
29 has a relatively high hold current while maintaining a very small circuit board

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1 footprint. This result is achieved by a multilayer construction that provides an
2 increased effective cross-sectional area A of the current flow path for a given
3 circuit board footprint. In effect, the multilayer construction of the invention
4 provides, in a single, small-footprint surface mount package, three or more
5 PTC devices electrically connected in parallel.

6 In one aspect, the present invention is a conductive polymer PTC
7 device comprising, in a preferred embodiment, multiple alternating layers of
8 metal foil and PTC conductive polymer material, with electrically conductive
9 interconnections to form three or more conductive polymer PTC devices
10 connected to each other in parallel, and with termination elements configured
11 for surface mount termination.

12 Specifically, two of the metal layers form, respectively, first and second
13 external electrodes, while the remaining metal layers form a plurality of
14 internal electrodes that physically separate and electrically connect three or
15 more conductive polymer layers located between the external electrodes. First
16 and second terminals are formed so as to be in physical contact with all of the
17 conductive polymer layers. The electrodes are staggered to create two sets of
18 alternating electrodes: a first set that is in electrical contact with the first
19 terminal, and a second set that is in electrical contact with the second terminal.
20 One of the terminals serves as an input terminal, and the other serves as an
21 output terminal.

22 A specific embodiment of the invention comprises first, second, and
23 third conductive polymer PTC layers. A first external electrode is in electrical
24 contact with the second terminal and with an exterior surface of the first
25 conductive polymer layer that is opposed to the surface facing the second
26 conductive polymer layer. A second external electrode is in electrical contact
27 with the first terminal and with an exterior surface of the third conductive
28 polymer layer that is opposed to the surface facing the second conductive
29 polymer layer. The first and second conductive polymer layers are separated

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1 by a first internal electrode that is in electrical contact with the first terminal,
2 while the second and third conductive polymer layers are separated by a
3 second internal electrode that is in electrical contact with the second terminal.

4 In such an embodiment, if the first terminal is an input terminal and the
5 second terminal is an output terminal, the current flow path is from the first
6 terminal to the first internal electrode and the second external electrode. From
7 the first internal electrode, current flows to the second terminal through the
8 first conductive polymer layer and the first external electrode, and through the
9 second conductive polymer layer and the second internal electrode. From the
10 second external electrode, current flows to the second terminal through the
11 third conductive polymer layer and the second internal electrode.

12 Thus, the resulting device is, effectively, three PTC devices connected
13 in parallel. This construction provides the advantages of a significantly
14 increased effective cross-sectional area for the current flow path, as compared
15 with a single layer device, without increasing the footprint. Thus, for a given
16 footprint, a larger hold current can be achieved.

17 A specific improvement of the present invention is characterized by a
18 fully-metallized external surface on each of the first and second external
19 electrodes to provide a large surface area for the adhesion of the upper and
20 lower ends of the first and second terminals to the first and second electrodes,
21 respectively. The improvement is further characterized by an external
22 insulation layer applied over the metallized external electrode surfaces
23 between the ends of the first and second terminals to provide electrical
24 isolation between the first and second terminals, wherein the external
25 insulation layer is flush with the upper and lower ends of the terminals.

26 The above-described improvement provides several advantages over
27 prior multilayer conductive polymer PCT devices, all stemming essentially
28 from the ability to provide a larger adhesion "patch" between the terminal ends
29 and the external electrodes. Specifically, this structure yields enhanced solder

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1 joint strength between the terminals and the external electrodes, enhanced heat
2 dissipation qualities, and lower contact resistance at the terminal junctures.
3 The latter two qualities, in turn, contribute to higher hold currents for a given
4 size device.

5 In another aspect, the present invention is a method of fabricating the
6 above-described device. For a device having three conductive polymer PTC
7 layers, this method comprises the steps of: (1) providing (a) a first laminated
8 substructure comprising a first conductive polymer PTC layer sandwiched
9 between first and second metal layers, (b) a second conductive polymer PTC
10 layer, and (c) a second laminated substructure comprising a third conductive
11 polymer PTC layer sandwiched between third and fourth metal layers; (2)
12 isolating selected areas of the second and third metal layers to form,
13 respectively, first and second internal arrays of internal metal strips; (3)
14 laminating the first and second laminated substructures to opposite surfaces of
15 the second conductive polymer PTC layer to form a laminated structure
16 comprising the first conductive polymer layer sandwiched between the first
17 and second metal layers, the second conductive polymer PTC layer
18 sandwiched between the second and third metal layers, and the third
19 conductive polymer PTC layer sandwiched between the third and fourth metal
20 layers; (4) isolating selected areas of the first and fourth metal layers to form,
21 respectively, first and second external arrays of external metal strips; (5)
22 forming a plurality of insulation areas on the exterior surfaces of each of the
23 external metal strips; and (6) forming a plurality of first terminals, each
24 electrically connecting one of the internal metal strips in the first internal array
25 to one of the external metal strips in the second external array, and a plurality
26 of second terminals, each electrically connecting one of the external metal
27 strips in the first external array to one of the internal metal strips in the second
28 internal array, wherein each of the first terminals is separated from a second
29 terminal by one of the insulation areas on each of the first and second external

1 arrays.

2 More specifically, the step of isolating selected areas of the second and
3 third metal layers includes the step of etching a series of parallel, linear
4 interior isolation gaps in each of the second and third metal layers to form first
5 and second internal arrays of isolated parallel metal strips. The interior
6 isolation gaps in the second and third metal layers are staggered so that the
7 isolated metal strips in the first internal array are staggered with respect to
8 those in the second internal array.

9 The step of isolating selected areas of the first and fourth metal layers
10 includes the steps of (a) forming a series of parallel linear slots through the
11 laminated structure, each of the slots passing through one of the interior
12 isolation gaps in either the second or third metal layer; (b) plating the side
13 walls of the slots and the exterior surfaces of the first and fourth metal layers
14 with a conductive metal plating; and (c) etching a series of parallel, linear
15 exterior isolation gaps in each of the first and fourth metal layers (including
16 the metal plating applied thereto), wherein the isolation gaps in the first metal
17 layer are adjacent a first set of slots, and the isolation gaps in the fourth metal
18 layer are adjacent a second set of slots that alternate with the first set. Thus,
19 the first external array of isolated metal strips comprises a first plurality of
20 wide external metal strips in the first metal layer, each defined between a slot
21 and an exterior isolation gap, while the second external array of isolated metal
22 strips comprises a second plurality of wide external metal strips in the fourth
23 metal layer, each defined between a slot and an external isolation gap, wherein
24 the wide external metal strips in the first array are on the opposite sides of the
25 slots from the wide external metal strips in the second array. Furthermore,
26 because of the asymmetric spacing of the isolation gaps between successive
27 slots, each isolation gap separates one of the wide external metal strips from a
28 narrow external metal band, and each slot has a narrow metal band on one side
29 and a wide metal strip on the other side.

1 The step of forming a plurality of insulation areas comprises the step of
2 screen printing a layer of insulation material on both of the external surfaces of
3 the laminated structure, along each of the wide external metal strips. The
4 insulation layers are applied so that the isolation gaps are filled with insulation
5 material, but a substantial portion of each of the wide external metal strips
6 along each of the slots is left uncovered or exposed. The narrow metal bands
7 are also left uncovered.

8 The step of forming the first and second terminals comprises the step of
9 overlaying a solder plating over the metal-plated surfaces that are not covered
10 by the insulation layer. The solder plating is thus applied to the interior wall
11 surfaces of the slots, the narrow external metal bands, and the exposed
12 portions of the wide external metal strips.

13 The final step of the fabrication process comprises the step of
14 singulating the laminated structure into a plurality of individual conductive
15 polymer PTC devices, each of which has the structure described above.
16 Specifically, the wide external metal strips in the first and fourth metal layers
17 are formed, by the singulation step, respectively into first and second
18 pluralities of external electrodes, while the isolated metal areas in the first and
19 second internal arrays are thereby respectively formed into first and second
20 pluralities of internal electrodes.

21 While a device having three conductive polymer PTC layers is
22 described herein, it will be appreciated that a device having two such layers, or
23 four or more such layers, can be constructed in accordance with the present
24 invention. Thus, the above-described fabrication method can be readily
25 modified to manufacture devices with two conductive polymer PTC layers, or
26 with four or more such layers.

27 The above-mentioned advantages of the present invention, as well as
28 others, will be more readily appreciated from the detailed description that
29 follows.

BRIEF DESCRIPTION OF THE DRAWINGS

Figure 1 is a cross-sectional view of the laminated substructures and a middle conductive polymer PTC layer, illustrating the first step of a conductive polymer PTC device fabrication method in accordance with a first preferred embodiment of the present invention;

Figure 2 is a top plan view of the first (upper) laminated substructure of Figure 1;

Figure 3 is a cross-sectional view, similar to that of Figure 1, after the performance of the step of creating first and second internal arrays of isolated metal areas respectively in the second and third metal layers of the laminated substructures of Figure 1;

Figure 3A is a plan view of the second metal layer, taken along line 3A - 3A of Figure 3;

Figure 3B is a plan view of the third metal layer, taken along line 3B - 3B of Figure 3;

Figure 3C is a cross-sectional view, similar to that of Figure 3, but showing the laminated structure formed after the lamination of the substructures and the middle conductive polymer PTC layer of Figure 3;

Figure 3D is a top plan view of the laminated structure of Figure 3C, showing the etched isolation gaps in the second and third metal layers in phantom outline;

Figure 4 is a top plan view of the laminated structure after the performance of the step of forming slots through the laminated structure;

Figure 5 is a cross-sectional view, taken along line 5 - 5 of Figure 4;

Figure 6 is a cross-sectional view, similar to that of Figure 5, after the performance of the step of metal-plating the side walls of the slots and the external surfaces of the laminated structure;

Figure 7 is a cross-sectional view similar to that of Figure 6, after the performance of the step of forming isolation gaps in the external surfaces of

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1 the laminated structure;

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2 Figure 8 is a cross-sectional, similar to that of Figure 7, after the
3 performance of the step of forming insulative isolation areas on the external
4 surfaces of the laminated structure;

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5 Figure 9 is a plan view of a portion of the laminated structure after the
6 performance of the step of forming the terminals;

7 Figure 10 is a cross-sectional view taken along line 10 - 10 of Figure 9;

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8 Figure 11 is a perspective view of a multilayer, conductive polymer
9 PTC device after singulation from the laminated structure; and

10 Figure 12 is a cross-sectional view taken along line 12 - 12 of Figure
11 11.

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12 DETAILED DESCRIPTION OF THE INVENTION

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13 Referring now to the drawings, Figure 1 illustrates a first laminated
14 substructure or web 10, and a second laminated substructure or web 12. The
15 first and second webs 10, 12 are provided as the initial step in the process of
16 fabricating a conductive polymer PTC device in accordance with the present
17 invention. The first laminated web 10 comprises a first layer 14 of conductive
18 polymer PTC material sandwiched between first and second metal layers 16a,
19 16b. A second or middle layer 18 of conductive polymer PTC material is
20 provided for lamination between the first web 10 and the second web 12 in a
21 subsequent step in the process, as will be described below. The second web 12
22 comprises a third layer 20 of conductive polymer PTC material sandwiched
23 between third and fourth metal layers 16c, 16d. The conductive polymer PTC
24 layers 14, 18, 20 may be made of any suitable conductive polymer PTC
25 composition, such as, for example, high density polyethylene (HDPE) into
26 which is mixed an amount of carbon black that results in the desired electrical
27 operating characteristics. See, for example, U.S. Patent No. 5,802,709 -
28 Hogge et al., , assigned to the assignee of the present invention, the disclosure
29 of which is incorporated herein by reference.

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1 The metal layers 16a, 16b, 16c, and 16d may be made of copper or
2 nickel foil, with nickel being preferred for the second and third (internal) metal
3 layers 16b, 16c. If the metal layers 16a, 16b, 16c, 16d are made of copper foil,
4 those foil surfaces that contact the conductive polymer layers are coated with a
5 nickel flash coating (not shown) to prevent unwanted chemical reactions
6 between the polymer and the copper. These polymer contacting surfaces are
7 also preferably "nodularized", by well-known techniques, to provide a
8 roughened surface that provides good adhesion between the metal and the
9 polymer. Thus, in the illustrated embodiment, the second and third (internal)
10 metal layers 16b, 16c are nodularized both surfaces, while the first and fourth
11 (external) metal layers 16a, 16d are nodularized only on the single surface that
12 contacts an adjacent conductive polymer layer.

13 The laminated webs 10, 12 may themselves be formed by any of
14 several suitable processes that are known in the art, as exemplified by U.S.
15 Patents Nos. 4,426,633 - Taylor; 5,089,801 - Chan et al.; 4,937,551 - Plasko;
16 and 4,787,135 - Nagahori, with the process disclosed in U.S. Patent No.
17 5,802,709 - Hogge et al. and International Publication No. WO97/06660 being
18 preferred.

19 It is advantageous at this point to provide some means for maintaining
20 the webs 10, 12 and the middle conductive polymer PTC polymer layer 18 in
21 the proper relative orientation or registration for carrying out the subsequent
22 steps in the fabrication process. Preferably, this is done by forming (e.g., by
23 punching or drilling) a plurality of registration holes 24 in the corners of the
24 webs 10, 12 and the middle polymer layer 18, as shown in Figure 2. Other
25 registration techniques, well known in the art, may also be used.

26 The next step in the process is illustrated in Figures 3, 3A, and 3B. In
27 this step, a pattern of metal in each of the second and third (internal) metal
28 layers 16b, 16c is removed to form first and second internal arrays of isolated
29 parallel metal strips 26b, 26c, respectively, in the internal metal layers 16b,

1 16c. Specifically, a first series of parallel, linear interior isolation gaps 28 is
2 formed in the second metal layer 16b, and a second series of parallel, linear
3 isolation gaps is formed in the third metal layer 16c, with the interior metal
4 strips 26b, 26c being defined between the interior isolation gaps 28 in the
5 second and third metal layers 16b, 16c, respectively. The metal removal to
6 form the gaps 28 is accomplished by means of standard techniques used in the
7 fabrication of printed circuit boards, such as those techniques employing
8 photoresist and etching methods. The removal of the metal results in a linear
9 isolation gap 28 between adjacent metal strips 26b, 26c in each of the internal
10 metal layers 16b, 16c. The interior isolation gaps 28 in the second and third
11 metal layers are staggered so that the isolated metal strips 26b in the first
12 internal array (in the second metal layer 16b) are staggered with respect to the
13 isolated metal strips 26c in the second internal array (in the third metal layer
14 16c).

15 Ensuring that the webs 10, 12 and the middle conductive polymer PTC
16 layer 18 are in proper registration, the middle conductive polymer PTC layer
17 18 is laminated between the webs 10, 12 by a suitable laminating method, as is
18 well known in the art. The lamination may be performed, for example, under
19 suitable pressure and at a temperature above the melting point of the
20 conductive polymer material, whereby the material of the conductive polymer
21 layers 14, 18, and 20 flows into and fills the isolation gaps 28. The laminate is
22 then cooled to below the melting point of the polymer while maintaining
23 pressure. The result is a laminated structure 30, as shown in Figures 3C and
24 3D. At this point, the polymeric material in the laminated structure 30 may be
25 cross-linked, by well-known methods, if desired for the particular application
26 in which the device will be employed.

27 After the laminated structure 30 has been formed, a series of parallel,
28 linear slots 32 is formed through the laminated structure 30, as shown in
29 Figures 4 and 5. The slots 32 may be formed by drilling, routing, or punching

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1 the laminated structure 30 completely through the four metal layers 16a, 16b,
2 16c, 16d, and the three polymer layers 14, 18, and 20. Each of the slots 32
3 passes through one of the interior isolation gaps 28 in either the second metal
4 layer 16b or the third metal layer 16c.

5 Next, as shown in Figure 6, the exposed exterior surfaces of the first
6 and fourth (external) metal layers 16a, 16d, and the interior wall surfaces of
7 the slots 32 are coated with a plating layer 34 of conductive metal, such as tin,
8 nickel, or copper, with copper being preferred. Alternatively, the plating layer
9 34 may comprise a layer of copper over a very thin base layer (not shown) of
10 nickel, for improved adhesion. This metal plating step can be performed by
11 any suitable process, such as electrodeposition, for example. The metal
12 plating layer 34 may be defined as having a first portion that is applied to the
13 interior wall surfaces of the slots 32, and second and third portions that are
14 applied to the external surfaces of the first and fourth metal layers 16a, 16d,
15 respectively.

16 Figure 7 illustrates the step of forming a series of parallel, linear
17 exterior isolation gaps 36 in each of the first and fourth metal layers 16a, 16d,
18 including the metal plating layer 34 applied thereto. The external isolation
19 gaps 36 in the first metal layer are adjacent a first set of slots 32, and the
20 external isolation gaps 36 in the fourth metal layer are adjacent a second set of
21 slots 32 that alternate with the first set. The exterior isolation gaps 36 may be
22 formed by the same process as that used to form the interior isolation gaps 28,
23 as discussed above.

24 The external isolation gaps 36 divide the first metal layer 16a into a
25 first plurality of external metal strips 38a, each defined between a slot 32 and
26 an exterior isolation gap 36, and they divide the fourth metal layer 16d into a
27 second plurality of external metal strips 38b in the fourth metal layer, each
28 defined between a slot 32 and an exterior isolation gap 36, wherein the
29 external metal strips 38a in the first array are on the opposite sides of the slots

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1 32 from the external strips 38b in the second array. Furthermore, because of
2 the asymmetric spacing of the external isolation gaps 36 between successive
3 slots 32, each external isolation gap 36 separates one of the external metal
4 strips 38a, 38b from a narrow external metal band 40a, 40b, respectively, and
5 each slot 32 has a narrow metal band 40a or 40b on one side and a metal strip
6 38a or 38b on the other side. Each of the metal strips 38a, 38b and the narrow
7 metal bands 40a, 40b comprises an inner foil layer and an outer metal-plated
8 layer.

9 Figure 8 illustrates the step of forming a plurality of insulation areas 42
10 on both of the major external surfaces (i.e., the top and bottom surfaces) of the
11 laminated structure 30. This step is advantageously performed by screen
12 printing a layer of insulation material on both of the appropriate surfaces of the
13 laminated structure 30, along each of the external metal strips 38a, 38b. The
14 insulation areas 42 are configured so that the external isolation gaps 36 are
15 filled with insulation material, but a substantial portion of each of the metal-
16 plated external metal strips 38a, 38b along each of the slots 32 is left
17 uncovered or exposed. Although the insulation areas 42 may cover a small
18 adjacent portion of the narrow bands 40a, 40b, most, if not all, of the surface
19 area of each of the narrow bands 40a, 40b is left uncovered by the insulation
20 layers 42.

21 Then, as shown in Figures 9 and 10, the areas that were metal-plated
22 with the plating layer 34 in the step discussed above in connection with Figure
23 6 are again plated with a thin solder coating 44. The solder coating 44, which
24 is preferably applied by electroplating, but which can be applied by any other
25 suitable process that is well-known in the art (e.g., reflow soldering or vacuum
26 deposition), covers the portion of the metal plating layer 34 that was applied to
27 the interior wall surfaces of the slots 32, and those portions of the external
28 strips 38a, 38b and the narrow metal bands 40a, 40b that are left uncovered by
29 the insulation layers 42. It is important that the solder coating 44 is flush with

the insulation layer 42. Therefore, the thicknesses of both the insulation layer 42 and the solder coating 44 must be controlled to assure that a substantially flush surface is provided on both the top and bottom surfaces of the laminated structure 30, as shown in Figure 10.

Finally, the laminated structure 30 is singulated (by well-known techniques) preferably along a grid of score lines (not shown) to form a plurality of individual conductive polymer PTC devices, one of which is shown in Figures 11 and 12, designated by the numeral 50. After singulation, the device includes a first external electrode 52, formed from one of the first external array of external metal strips 38a; a first internal electrode 54, formed from one of the first internal array of internal metal strips 26b; a second internal electrode 56, formed from one of the second array of internal metal strips 26c; and a second external electrode 58, formed from one of the second array of external metal strips 38b. A first conductive polymer PTC element 60, formed from the first polymer layer 14, is located between the first external electrode 52 and the first internal electrode 54; a second conductive polymer PTC element 62, formed from the second polymer layer 18, is located between the first internal electrode 54 and the second internal electrode 56; and a third conductive polymer PTC element 64, formed from the third polymer layer 20, is located between the second internal electrode 56 and the second external electrode 58.

The solder plating layer 44, described above, provides first and second conductive terminals 66, 68 on opposite ends of the device 50. The first and second terminals 66, 68 form the entire end surfaces and parts of the top and bottom surfaces of the device 50. The remaining portions of the top and bottom surfaces of the device 50 are formed by the insulation layers 42, which electrically isolate the first and second terminals 66, 68 from each other.

As best seen in Figure 12, the first terminal 66 is in intimate physical contact with the first internal electrode 54 and the second external electrode

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1 58. The second terminal 58 is in intimate physical contact with the first
2 external electrode 52d and the second internal electrode 56. The first terminal
3 66 is also in contact with a top metal segment 70a, which is formed from one
4 of the above-described narrow metal bands 40a, while the second terminal 68
5 is in contact with a second metal segment 70b, which is formed from the other
6 of the narrow metal bands 40b. The metal segments 70a, 70b are of such
7 small area as to have a negligible current-carrying capacity, and thus do not
8 function as electrodes, as will be seen below.

9 For the purposes of this description, the first terminal 66 may be
10 considered an input terminal, and the second terminal 68 may be considered an
11 output terminal, but these assigned roles are arbitrary, and the opposite
12 arrangement may be employed. With the terminals 66, 68 so defined, the
13 current path through the device 50 is as follows: From the input terminal 66
14 current flows (a) through the first internal electrode 54, the first conductive
15 polymer PTC layer 14, and the first external electrode 52 to the output
16 terminal 68; (b) through the first internal electrode 54, the second conductive
17 polymer PTC layer 18, and the second internal electrode 56, to the output
18 terminal 68; and (c) through the second external electrode 58, the third
19 conductive polymer PTC layer 20 and the second internal electrode 56, to the
20 output terminal 68. This current flow path is equivalent to connecting the
21 conductive polymer PTC layers 14, 18, and 20 in parallel between the input
22 and output terminals 66, 68.

23 It will be appreciated that the device constructed in accordance with the
24 above described fabrication process is very compact, with a small footprint,
25 and yet it can achieve relatively high hold currents.

26 The device 50 in accordance with the present invention is characterized
27 by the fully-metallized layer 34 on the surface on each of the first and second
28 external electrodes 52, 58 to provide a large surface area for the adhesion of
29 the upper and lower ends of the first and second terminals 66, 68 on the upper

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1 and lower surfaces, respectively, of the device 50. The improvement is further
2 characterized by the external insulation layer 42 applied over the metallized
3 external surfaces of the external electrodes 52, 58, between the ends of the first
4 and second terminals 66, 68, to provide electrical isolation between the first
5 and second terminals 66, 68, wherein the external insulation layer 42 is flush
6 with the solder plating of the terminals 66, 68 on the upper and lower surfaces
7 of the device 50.

8 The above-described improvement provides several advantages over
9 prior multilayer conductive polymer PTC devices, all stemming essentially
10 from the ability to provide a larger adhesion "patch" between the terminal ends
11 and the external electrodes 52, 58. Specifically, this structure yields enhanced
12 solder joint strength between the terminals 66, 68 and the external electrodes
13 52, 58, enhanced heat dissipation qualities, and lower contact resistance at the
14 terminal junctures. The latter two qualities, in turn, contribute to higher hold
15 currents for a given size device. Of significant importance is that a larger area
16 of overlap is provided between successive electrodes than has heretofore been
17 achieved in a multilayer polymer PTC device, thereby increasing the effective
18 current-carrying cross-sectional area of the device. This, in turn, further
19 increases the hold current for a given footprint.

20 It will be appreciated that the fabrication method described above may
21 be easily modified to manufacture a device comprising a single conductive
22 polymer layer sandwiched between two electrodes, with a terminal electrically
23 connected to each electrode, the terminals being electrically isolated from each
24 other by insulation layers on the upper and lower exterior surfaces of the
25 device. Specifically, such a method would comprise the steps of: (1)
26 providing a laminated structure comprising a first conductive polymer layer
27 sandwiched between first and second metal layers; (2) isolating selected areas
28 of the first and second metal layers to form, respectively, first and second
29 arrays of metal strips; (3) forming a first plurality of insulation areas on the

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1 exterior surface of each of the first array of metal strips and a second plurality
2 of insulation areas on the exterior surface of each of the second array of metal
3 strips; (4) forming a plurality of first terminals, each electrically connected to
4 one of the metal strips in the first array, and a plurality of corresponding
5 second terminals, each electrically connected to one of the metal strips in the
6 second array, each of the first terminals being isolated from a corresponding
7 second terminal by one of the first plurality of insulation areas and one of the
8 second plurality of insulation areas; and (5) separating the laminated structure
9 into a plurality of devices, each comprising a conductive polymer layer
10 sandwiched between a first electrode formed from one of the metal strips in
11 the first array and a second electrode formed from one of the metal strips in
12 the second array; a first terminal in electrical contact only with the first
13 electrode; and a second terminal in electrical contact only with the second
14 electrode.

15 In the single layer embodiment, the step of isolating selected areas of
16 the first and second metal layers comprises the steps of: (2)(a) forming a series
17 of substantially parallel linear slots through the laminated structure; (2)(b)
18 plating the internal side walls of the slots and the exterior surfaces of the first
19 and second metal layers with a conductive metal plating layer; and (2)(c)
20 etching a series of substantially linear isolation gaps in each of the first and
21 second metal layers, including the metal plating layer applied thereto. The
22 steps of forming the insulation areas and forming the terminals would be
23 performed substantially as described above with respect to the multilayer
24 embodiment, with the proviso that the terminals are formed so that each of the
25 first plurality of terminals electrically contacts only the first electrode, and
26 each of the second plurality of terminals contacts only the second electrode.

27 While exemplary embodiments have been described in detail in this
28 specification and in the drawings, it will be appreciated that a number of
29 modifications and variations may suggest themselves to those skilled in the

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1 pertinent arts. For example, the fabrication process described herein may be
2 employed with conductive polymer compositions of a wide variety of
3 electrical characteristics, and is thus not limited to those exhibiting PTC
4 behavior. It will also be readily apparent that the fabrication method described
5 above may be easily adapted to the manufacture of a device having fewer than
6 three or more than three conductive polymer layers. Furthermore, while the
7 present invention is most advantageous in the fabrication of SMT devices, it
8 may be readily adapted to the fabrication of multilayer conductive polymer
9 devices having a wide variety of physical configurations and board mounting
10 arrangements. These and other variations and modifications are considered
11 the equivalents of the corresponding structures or process steps explicitly
12 described herein, and thus are within the scope of the invention as defined in
13 the claims that follow.

Claims

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1 WHAT IS CLAIMED IS:

2 1. A method of fabricating an electronic device, comprising the steps
10 3 of:

4 (1) providing (a) a first laminated substructure comprising a first
5 conductive polymer layer sandwiched between first and second metal layers,
15 6 (b) a second conductive polymer layer, and (c) a second laminated
7 substructure comprising a third conductive polymer layer sandwiched between
8 third and fourth metal layers;

9 (2) isolating selected areas of the second and third metal layers to form,
20 10 respectively, first and second internal arrays of internal metal strips;

11 (3) laminating the first and second laminated substructures to opposite
12 surfaces of the second conductive polymer layer to form a laminated structure;

25 13 (4) isolating selected areas of the first and fourth metal layers to form,
14 respectively, first and second external arrays of external metal strips;

15 (5) forming a plurality of insulation areas on the exterior surfaces of
30 16 each of the external metal strips; and

17 (6) forming a plurality of first terminals, each electrically connecting
18 one of the internal metal strips in the first internal array to one of the external
35 19 metal strips in the second external array, and a plurality of second terminals,
20 each electrically connecting one of the external metal strips in the first external
21 array to one of the internal metal strips in the second internal array.

40 22 2. The method of Claim 1, wherein the conductive polymer exhibits
23 PTC behavior.

24 3. The method of Claim 1, wherein the metal layers are made of a
45 25 material selected from the group consisting of nickel foil and nickel-coated
26 copper foil.

27 4. The method of Claims 1, 2, or 3, further comprising the step of:

50 28 (7) separating the laminated structure into a plurality of devices, each
29 comprising:

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1 a first conductive polymer layer sandwiched between a first external
2 electrode formed from one of the external metal strips in the first external
3 array and a first internal electrode formed from one of the internal metal strips
4 in the first internal array;

5 a second conductive polymer layer sandwiched between the first
6 internal electrode and a second internal electrode formed from one of the
7 internal metal strips in the second internal array; and

8 a third conductive polymer layer sandwiched between the second
9 internal electrode and a second external electrode formed from one of the
10 external metal strips in the second external array;

11 wherein the first terminal is in electrical contact only with the first
12 internal electrode and the second external electrode, and the second terminal is
13 in electrical contact only with the first external electrode and the second
14 internal electrode.

15 5. The method of Claims 1, 2, or 3, wherein the step of isolating
16 selected areas of the second and third metal layers comprises the step of
17 etching a series of substantially parallel linear isolation gaps in each of the
18 second and third metal layers to form the first and second internal arrays of
19 internal metal strips.

20 6. The method of Claim 5, wherein the isolation gaps in the second and
21 third metal layers are staggered relative to each other so that the internal metal
22 strips in the first internal array are staggered with respect to the internal metal
23 strips in the second internal array.

24 7. The method of Claim 6, wherein the step of isolating selected areas
25 of the first and fourth metal layers comprises the steps of: (4)(a)
26 forming a series of substantially parallel linear slots through the laminated
27 structure, each of the slots passing through one of the interior isolation gaps in
28 either the second or third metal layer;

29 (4)(b) plating the internal side walls of the slots and the exterior

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1 surfaces of the first and fourth metal layers with a conductive metal plating
2 layer; and

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3 (4)(c) etching a series of substantially linear external isolation gaps in
4 each of the first and fourth metal layers, including the metal plating layer
5 applied thereto.

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6 8. The method of Claim 7, wherein the step of etching a series of
7 external isolation gaps is performed so that the external isolation gaps that are
8 formed in the first metal layer are adjacent a first set of the slots, and the
9 external isolation gaps that are formed in the fourth metal layer are adjacent a
10 second set of the slots that alternate with the first set.

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11 9. The method of Claim 7, wherein the step of forming the plurality of
12 insulation areas comprises the step of depositing a layer of insulation material
13 over the conductive metal plating layer on the exterior surfaces of the first and
14 fourth metal layers so as to fill in the external isolation gaps with the insulation
15 material, and so as to leave portions of the first and fourth metal layers
16 adjacent each of the slots with exposed metal plating from the plating step.

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17 10. The method of Claim 9, wherein the step of forming the pluralities
18 of first and second terminals comprises the step of depositing a solder layer on
19 the plated internal walls of the slots and on the portions of the first and fourth
20 metal layers with exposed metal plating.

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21 11. The method of Claim 10, wherein the step of depositing the solder
22 layer is performed so that the portion of the solder layer that is deposited on
23 the first and fourth metal layers is substantially flush with the layer of
24 insulation material.

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25 12. An electronic device having first and second opposed end surfaces,
26 the device comprising:

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27 first, second, and third conductive polymer layers, each having first and
28 second opposed surfaces;

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29 the first and second conductive polymer layers being separated by a

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1 first internal electrode that is in electrical contact with the second surface of
2 the first conductive polymer layer and with the first surface of the second
3 conductive polymer layer;

4 the second and third conductive polymer layers being separated by a
5 second internal electrode that is in electrical contact with the second surface
6 of the second conductive polymer layer and with the first surface of the third
7 conductive polymer layer;

8 a first external electrode having an internal surface in electrical contact
9 with the first surface of the first conductive polymer layer and an external
10 surface;

11 a second external electrode having an internal surface in electrical
12 contact with the second surface of the third conductive polymer layer and an
13 external surface;

14 a conductive metal layer having a first and second end portions
15 respectively covering the first and second end surfaces of the device so as to
16 be in electrical contact with the first and second internal electrodes,
17 respectively, and top and bottom portions respectively covering the external
18 surfaces of the first and second external electrodes;

19 a first terminal formed over the first end portion and part of the bottom
20 portion of the conductive metal layer so as to be in electrical contact with the
21 first internal electrode and with the second external electrode; and

22 a second terminal formed over the second end portion and part of the
23 top portion of the metal layer so as to be in electrical contact with the second
24 internal electrode and the first external electrode.

25 13. The electronic device of Claim 12, wherein the electrode elements
26 are made of a metal foil.

27 14. The electronic device of Claim 13, wherein the metal foil is made
28 of a material selected from the group consisting of nickel and nickel-coated
29 copper.

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1 15. The electronic device of Claim 12, wherein the first, second, and
2 third conductive polymer layers are made of a material that exhibits PTC
3 behavior.

4 16. The electronic device of Claim 12, wherein the first and second
5 terminals are formed by a solder layer applied over the conductive metal layer.

6 17. The electronic device of Claims 12, 13, 14, 15, or 16, further
7 comprising:

8 an insulative layer on each of the top and bottom portions of the
9 conductive metal layer and located so as to insulate the first and second
10 terminals from each other.

11 18. The electronic device of Claim 17, wherein the first and second
12 terminals and the top and bottom portions of the conductive metal layer define
13 substantially flush top and bottom surfaces of the device.

14 19. The electronic device of Claims 12, 13, 14, 15, or 16, wherein the
15 first, second, and third conductive polymer layers are connected in parallel
16 between the first and second terminals by the first and second internal
17 electrodes and the first and second external electrodes.

18 20. A method of fabricating an electronic device, comprising the steps
19 of:

20 (1) providing a laminated structure comprising a first conductive
21 polymer layer sandwiched between first and second metal layers;

22 (2) isolating selected areas of the first and second metal layers to form,
23 respectively, first and second arrays of metal strips;

24 (3) forming a first plurality of insulation areas on the exterior surface of
25 each of the first array of metal strips and a second plurality of insulation areas
26 on the exterior surface of each of the second array of metal strips; and

27 (4) forming a plurality of first terminals, each electrically connected to
28 one of the metal strips in the first array, and a plurality of corresponding
29 second terminals, each electrically connected to one of the metal strips in the

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1 second array, each of the first terminals being isolated from a corresponding
2 second terminal by one of the first plurality of insulation areas and one of the
3 second plurality of insulation areas.

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4 21. The method of Claim 20, wherein the conductive polymer exhibits
5 PTC behavior.

6 22. The method of Claim 20, wherein the metal layers are made of a
7 material selected from the group consisting of nickel foil and nickel-coated
8 copper foil.

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9 23. The method of Claims 20, 21, or 22, further comprising the step of:
10 (5) separating the laminated structure into a plurality of devices, each
11 comprising:

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12 a conductive polymer layer sandwiched between a first electrode
13 formed from one of the metal strips in the first array and a second electrode
14 formed from one of the metal strips in the second array;

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15 a first terminal in electrical contact only with the first electrode; and
16 a second terminal in electrical contact only with the second electrode.

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17 24. The method of Claims 20, 21, or 22, wherein the step of isolating
18 selected areas of the first and second metal layers comprises the steps of:

19 (2)(a) forming a series of substantially parallel linear slots through the
20 laminated structure;

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21 (2)(b) plating the internal side walls of the slots and the exterior
22 surfaces of the first and second metal layers with a conductive metal plating
23 layer; and

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24 (2)(c) etching a series of substantially linear isolation gaps in each of
25 the first and second metal layers, including the metal plating layer applied
26 thereto.

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27 25. The method of Claim 24, wherein the step of etching a series of
28 isolation gaps is performed so that the isolation gaps that are formed in the
29 first metal layer are adjacent a first set of the slots, and the isolation gaps that

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1 are formed in the second metal layer are adjacent a second set of the slots that
2 alternate with the first set.

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3 26. The method of Claim 24, wherein the step of forming the first and
4 second pluralities of insulation areas comprises the step of depositing first and
5 second layers of insulation material over the conductive metal plating layer on
6 the exterior surface of the first and second metal layers, respectively, so as to
7 fill in the isolation gaps with the insulation material, and so as to leave
8 portions of the first and second metal layers adjacent each of the slots with
9 exposed metal plating from the plating step.

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10 27. The method of Claim 26, wherein the step of forming the
11 pluralities of first and second terminals comprises the step of depositing a
12 solder layer on the plated internal walls of the slots and on the portions of the
13 first and second metal layers with exposed metal plating.

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14 28. The method of Claim 27, wherein the step of depositing the solder
15 layer is performed so that the portion of the solder layer that is deposited on
16 the first and second metal layers is substantially flush with the layer of
17 insulation material.

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18 29. An electronic device having first and second opposed end surfaces,
19 the device comprising:

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20 a conductive polymer layer having first and second opposed surfaces;

21 a first electrode having an internal surface in electrical contact with the
22 first surface of the conductive polymer layer and an external surface;

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23 a second electrode having an internal surface in electrical contact with
24 the second surface of the conductive polymer layer and an external surface;

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25 a conductive metal layer having a first and second end portions
26 respectively covering the first and second end surfaces of the device, and top
27 and bottom portions respectively covering the external surfaces of the first and
28 second electrodes;

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29 a first terminal formed over the first end portion and part of the bottom

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5

29

1 portion of the conductive metal layer so as to be in electrical contact with the
2 second electrode; and

10

3 a second terminal formed over the second end portion and part of the
4 top portion of the metal layer so as to be in electrical contact with the first
5 electrode.

15

6 30. The electronic device of Claim 29, wherein the electrode elements
7 are made of a metal foil.

20

8 31. The electronic device of Claim 30, wherein the metal foil is made
9 of a material selected from the group consisting of nickel and nickel-coated
10 copper.

25

11 32. The electronic device of Claim 29, wherein the conductive polymer
12 layer is made of a material that exhibits PTC behavior.

13 33. The electronic device of Claim 29, wherein the first and second
14 terminals are formed by a solder layer applied over the conductive metal layer.

30

15 34. The electronic device of Claims 29, 30, 31, 32, or 33, further
16 comprising:

35

17 an insulative layer on each of the top and bottom portions of the
18 conductive metal layer and located so as to insulate the first and second
19 terminals from each other.

40

20 35. The electronic device of Claim 34, wherein the first and second
21 terminals and the top and bottom portions of the conductive metal layer define
22 substantially flush top and bottom surfaces of the device.

45

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55

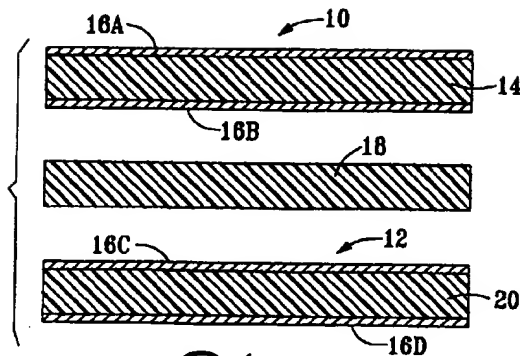


Fig. 1

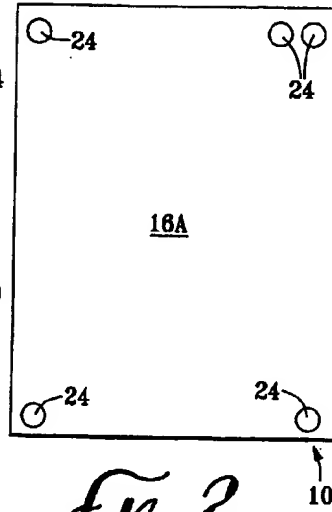


Fig. 2

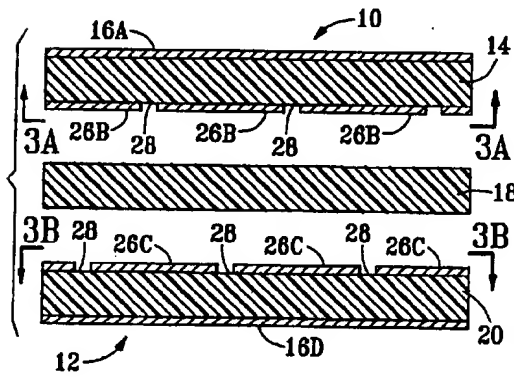


Fig. 3

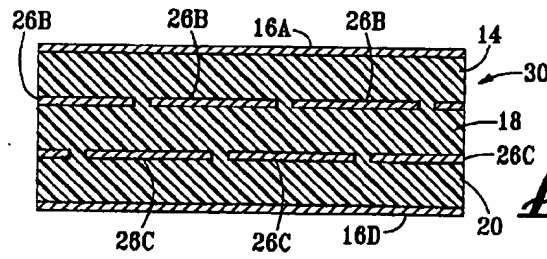


Fig. 3C

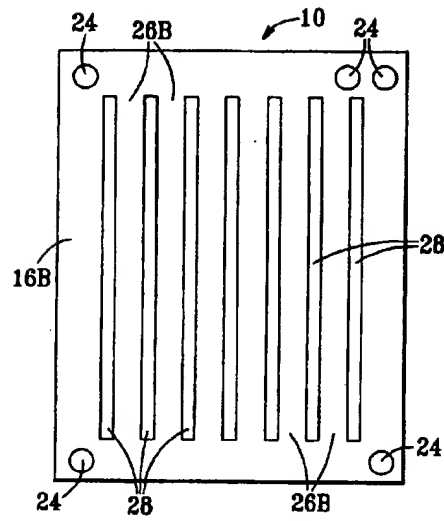


FIG. 3A

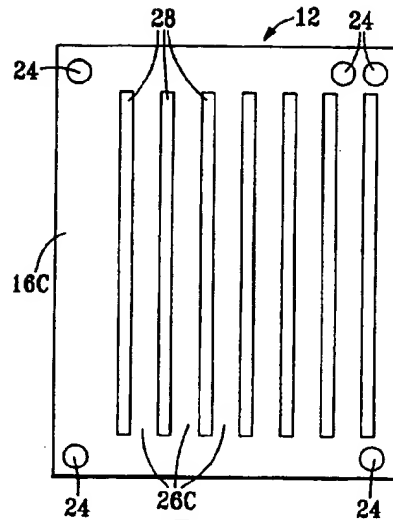


FIG. 3B

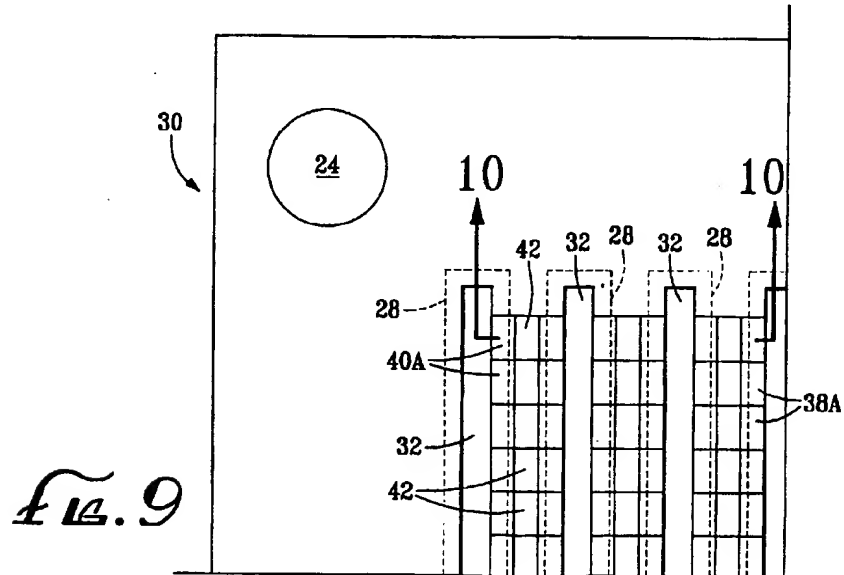
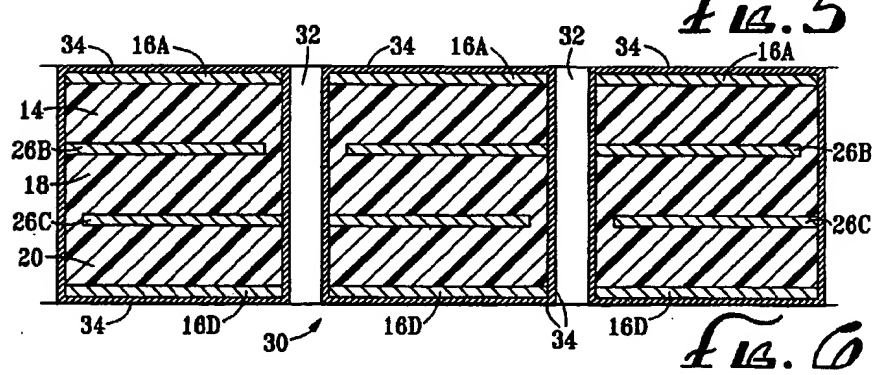
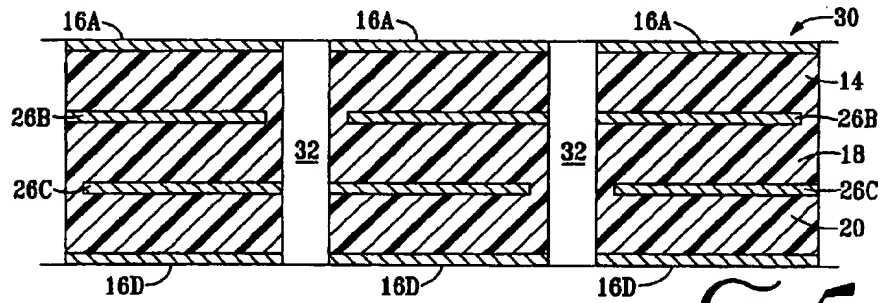
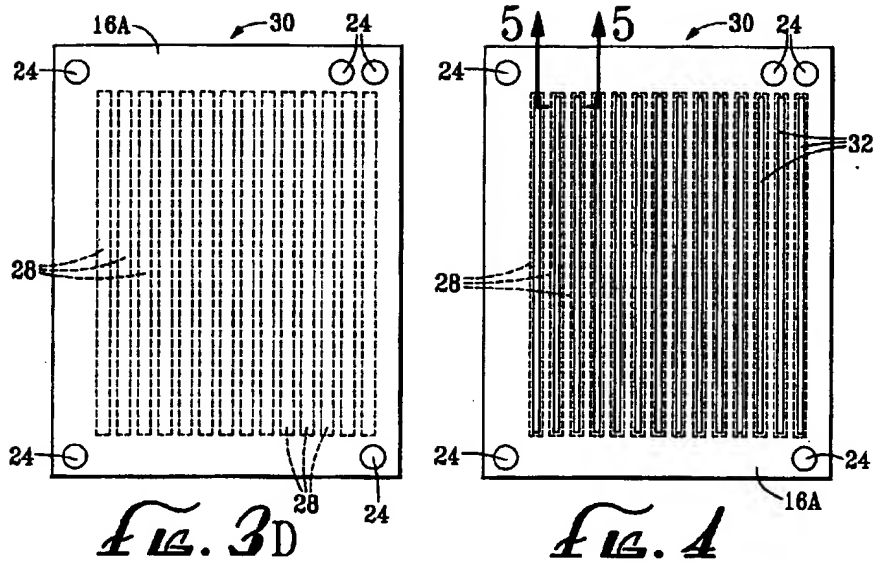
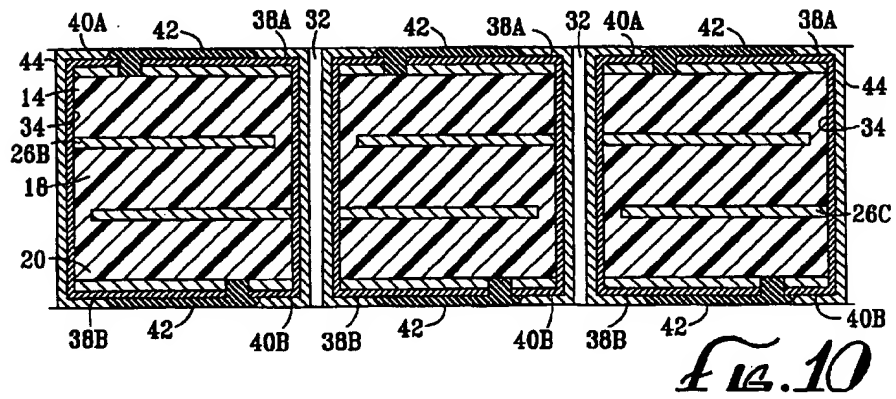
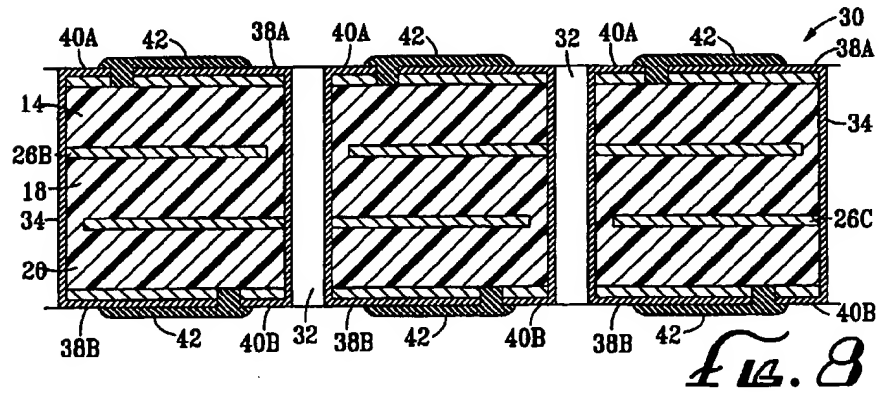
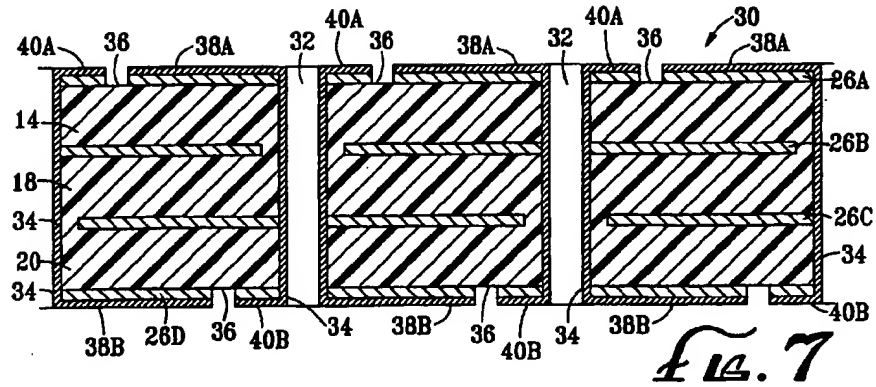


FIG. 9





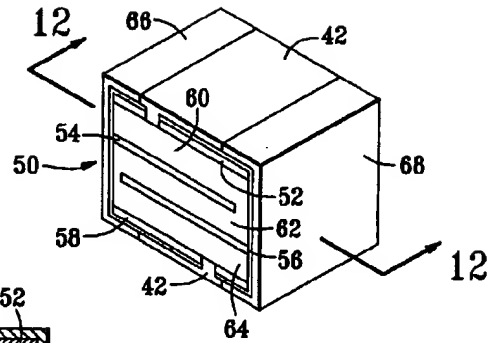


Fig. 11

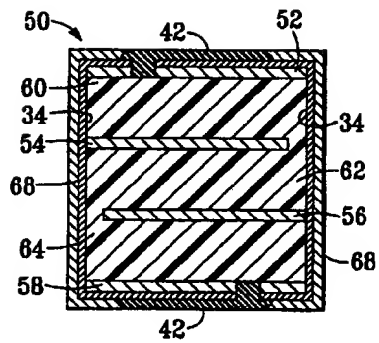


Fig. 12

INTERNATIONAL SEARCH REPORT

International Application No.

PCT/US 99/29416

A. CLASSIFICATION OF SUBJECT MATTER

IPC 7 H01C7/02

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

IPC 7 H01C

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the International search (name of data base and, where practical, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

| Category * | Citation of document, with indication, where appropriate, of the relevant passages | Relevant to claim No. |
|------------|--|-------------------------|
| Y | WO 95 31816 A (RAYCHEM CORP) 23 November 1995 (1995-11-23) | 1-3, 12-22, 29-35 |
| A | page 12, paragraph 2; claims 1,3,7 | 4,23 |
| Y | US 5 493 266 A (SASAKI KIYOMI ET AL) 20 February 1996 (1996-02-20) | 1-3, 12-22, 29-35 |
| A | claims 1,2; figures 2,3 PATENT ABSTRACTS OF JAPAN vol. 013, no. 280 (E-779), 27 June 1989 (1989-06-27) & JP 01 066903 A (MURATA MFG CO LTD), 13 March 1989 (1989-03-13) abstract | 1,12,20, 29 |



Further documents are listed in the continuation of box C.



Patent family members are listed in annex.

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"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art.

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Date of the actual completion of the international search

20 March 2000

Date of mailing of the international search report

31/03/2000

Name and mailing address of the ISA

European Patent Office, P.O. Box 6618 Petersenstr. 2
NL - 2280 HV Rijswijk
Tel. (+31-70) 540-2040, Tlx. 31 651 601
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Odgers, M

INTERNATIONAL SEARCH REPORT

information on patent family members

International Application No.

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| Patent document cited in search report | Publication date | Patent family member(s) | Publication date |
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| JP 01066903 A | 13-03-1989 | NONE | |